REMARKS/ARGUMENTS

Reconsideration of the application, in view of the above amendments and the following remarks, is respectfully requested.

The Examiner rejects Claims 1-2, 8-11 and 13-22 under 35 U.S.C. 103(a) as being unpatentable over Marshall et al in view of Avasarala et al. The Examiner states that Marshall teaches a transceiver coupled to receive a signal at a first node between 114 and 110, circuitry 104 (sic 114) or 112 coupled to establish the desired common mode voltage at a second node between 112 and 108; a transmitter coupled to provide an output signal at a third node between Tx and 108 which is different from the first and second nodes; the first and second nodes defining at least a portion of a low impedance path during a first operating mode for diverting a signal received at the first node from the receiver and a high impedance path during a second mode. The Examiner states that Marshall fails to teach the first and second nodes being disconnected but that Avarsala teaches first (line to receiver 212) and second (line to transmitter) nodes being disconnected and concludes that it would have been obvious what Marshall fails to teach that is taught by Avarsala into Marshall's transceiver in order to reduce interference.

We can not agree. First of all, Marshall does not show 3 nodes, the Examiner's statements to the contrary notwithstanding. The output of the transmitter Tx and the connection of the switch are but a single node. One can not use the spacing of elements in patent drawings to determine separation of parts. These are schematic drawings only and are drawn to Office specifications as to the size of elements and spacing of the elements so that the drawings are clear. The 2 "nodes" referred to by the Examiner are connected by a line in the drawings and are at the same voltage. Enclosed is a definition of the term of art "node" so that the Examiner can see that only a single node exists in Marshall et al.

Secondly, in Marshall et al, the switches 112,114 are mechanically linked so that one always is closed and the other open at any given time. Thus, the switches are not utilized as the Examiner describes.

Furthermore, Marshall et al does not have circuitry to maintain a common mode voltage at the ends of the switch as in the present invention. Note that in Figs. 3,4 switch 112 is connected to ground whereas switch 114 is connected to Vc. There is no showing or suggestion of the amplifiers 104,106 being connected to a reference to provide the common mode voltage, nor are differential inputs shown which could provide a common mode voltage; both amplifiers are single-ended. In addition, the input to the receiver 106 in Figs. 3,4 has a capacitor 302 in series with the input to the receiver. How can the receiver 106 provide the common mode voltage when its input is only AC coupled? Applicants are enclosing herewith a definition from the IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition for the term "common mode voltage" so that the Examiner can see that this term of art is not being properly applied in the rejection.

Avasarala et al shows the connection and disconnection of a second antenna which is used for transmitting in a first mode and as a diversity antenna in a second mode. It does not show or suggest using the switch to bypass energy from the transmitter from being input to the receiver in the transmit mode, the Examiner's statements to the contrary notwithstanding. In the transmit mode the switch is in its high impedance state to block the flow of the transmitter signal from the receiver input. In the present invention the switch is in its low impedance state during transmitting to shunt the signal away from the receiver input, just the opposite of what is done in Avarsala et al.

The Examiner states that one can not argue the differences of single references individually in a combination of references rejection. Applicants do not believe that is

what was done in the previous response. However, to be clear, combining these 2 references does not show or suggest the present invention. Avarsala et al if combined with Marshall et al would have the switch connecting an antenna in the receive mode of operation and have the switch open during the transmit mode. This is not how the present invention works or how it is claimed. Furthermore, Avarsala et al does not overcome the lack of showing or suggestion of a common mode voltage on both ends of the switch because this is not discussed or suggested by either reference. As to the Examiner's statement for the motivation to apply Avarsala et al's teaching to Marshall et al, to avoid interference, this would mean disconnecting the receiver from the transmitter output in order to avoid the interference created by receiving the output (transmitted) signal. Again, that is the opposite of the present invention.

The Examiner states that apparatus Claim 14 is rejected for the same reason as Claim 1 since the recited elements would perform the claimed steps.

This rejection is respectfully traversed. Claim 14 is an apparatus claim and does not recite steps. Accordingly, this rejection is inappropriate and should be withdrawn.

The Examiner rejects Claim 3 under 35 U.S.C. 103(a) as being unpatentable over Marshall et al in view of Avarsala et al. Claim 3 is now dependant on Claim 1. The patentability of Claim 1 having been shown above, Claim 3 is patentable for the same reasons.

The Examiner rejects Claims 4-6 and 12 under 35 U.S.C. 103(a) as being unpatentable over Marshall et al in view of Avarsal et al and further in view of Kim et al. Claims 4-6 are dependant directly or indirectly from Claim1. The patentabilty of Claim 1 having been shown above, they are patentable for the same reasons. Claim 12 is now dependant

on Claim 11. The patentabilty of Claim 11 having been shown above, this claim is patentable for the same reasons.

Claim 1 has been amended to recite the shared antenna and to define the operation of the switch. Claim 11 has been amended to recite the mitigation of transients by having the same common mode voltage at both ends of the switch. Claims 12 and 13 have been made dependant on Claim 11 and some formal amendments to the claims have been made. Claim 21 was cancelled without prejudice and Claim 22 made dependant on Claim 18. Claims 2, 7, 8 were cancelled without prejudice.

Accordingly, Applicants believe that the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted

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IEEE Std 100-1996

The IEEE Standard Dictionary of Electrical and Electronics Terms

Sixth Edition

Standards Coordinating Committee 10, Terms and Definitions
Jane Radatz, Chair

This standard is one of a number of information technology dictionaries being developed by standards organizations accredited by the American National Standards Institute. This dictionary was developed under the sponsorship of voluntary standards organizations, using a consensus-based process.

ISBN 1-55937-833-6
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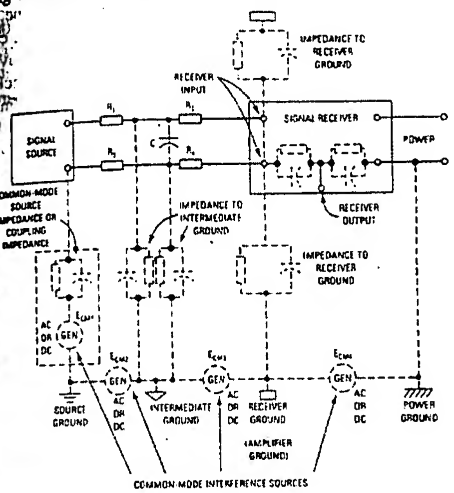
common-mode failure (nuclear power generating station) (safety systems equipment in nuclear power generating stations) Multiple failures attributable to a common cause. (PE/SWG) 308-1980s, 627-1980r, 649-1980s, 650-1979s, C37.100-1992

common-mode interference (1) (automatic null-balanced electrical instruments) Interference that appears between both signal leads and a common reference plane (ground) and causes the potential of both sides of the transmission path to be changed simultaneously and by the same amount relative to the common reference plane (ground). *See also:* interference. (EMC/IE/PE/SUB) [43], C37.1-1994, C63.13-1991
(2) A form of interference that appears between any measuring circuit terminal and ground. *See also:* accuracy rating.



Common-mode interference sources and current paths. The common-mode voltage V_{CM} in any path is equal to the sum of the common-mode generator voltages in that path; for example, in the source-receiver path.

$$V_{CM} = E_{CM1} + E_{CM2} + E_{CM3}.$$

common-mode interference

(EEC/PE/SUB) [112], C37.1-1994

common-mode noise (cable systems in power generating stations) (longitudinal) The noise voltage that appears equally and in phase from each signal conductor to ground. Common mode noise may be caused by one or more of the following:

a) Electrostatic induction. With equal capacitance between the signal wires and the surroundings, the noise voltage developed will be the same on both signal wires.
b) Electromagnetic induction. With the magnetic field linking the signal wires equally, the noise voltage developed will be the same on both signal wires.

(IA/PE/SUB) 1050-1996, 1100-1992, 1143-1994, 422-1977, 525-1992

common-mode outage *See:* common-mode outage event.

common-mode outage event A related multiple outage event consisting of two or more primary outage occurrences initiated by a single incident or underlying cause where the outage occurrences are not consequences of each other. *Note:* Primary outage occurrences in a common-mode outage event are referred to as common-mode outage occurrences or simply common-mode outages. Examples of common-mode outage events are a single lightning stroke causing tripouts of both circuits on a common tower, and an external object causing the outage of two circuits on the same right-of-way. *See also:* related multiple outage event. (PE) 859-1987r

common-mode overvoltage A signal level whose magnitude is less than the specified maximum safe common-mode signal but greater than the maximum operating common-mode signal. (IM) 1057-1994

common-mode overvoltage recovery time The time required for the recorder to return to its specified characteristics after the end of a common-mode overvoltage pulse. (IM) 1057-1994

common-mode radio noise Conducted radio noise that appears between a common reference plane (ground) and all wires of a transmission line causing their potentials to be changed simultaneously and by the same amount relative to the common reference plane (ground). (EMC) C63.4-1991

common-mode rejection (in-phase rejection) The ability of certain amplifiers to cancel a common-mode signal while responding to an out-of-phase signal. (EMB) [47]

common-mode rejection quotient (in-phase rejection quotient) The quotient obtained by dividing the response to a signal applied differentially by the response to the same signal applied in common mode, or the relative magnitude of a common-mode signal that produces the same differential response as a standard differential input signal. (EMB) [47]

common-mode rejection ratio (CMRR) (1) (signal-transmission signal) The ratio of the common-mode interference voltage at the input terminals of the system to the effect produced by the common-mode interference, referred to the input terminals for an amplifier. For example,

$$\mathrm{CMRR} = \frac{V_{CM}\text{ (root-mean-square) at input}}{\text{effect at output/amplifier gain}}$$

See also: interference. (IE) [43]
(2) **(oscilloscopes)** The ratio of the deflection factor for a common-mode signal to the deflection factor for a differential signal applied to a balanced-circuit input. *See also:* oscillograph. (Std100)
(3) The ratio of the input common-mode signal to the effect produced at the output of the recorder in units of the input. (IM) 1057-1994

common mode signal The average value of the signals at the positive and negative inputs of a differential input waveform recorder. If the signal at the positive input is designated V_+, and the signal at the negative input is designated V_-, then the common mode signal (V_{cm}) is

$$V_{cm} = \frac{V+ + V-}{2}$$

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common-mode to normal-mode conversion In addition to the common-mode voltages which are developed in the single conductors by the general environmental sources of electrostatic and electromagnetic fields, differences in voltage exist between different ground points in a facility due to the flow of ground currents. These voltage differences are considered common mode when connection is made to them either intentionally or accidentally, and the currents they produce are common mode. These common-mode currents can develop normal-mode noise voltage across unequal circuit impedances. (PE/SUB) 422-1977, 525-1992

common-mode voltage (1) The voltage that, at a given location, appears equally and in phase from each signal conductor to ground. (PE) C37.90.1-1989r
(2) The instantaneous algebraic average of two signals applied to a balanced circuit, with both signals referenced to a common reference. *Synonym:* longitudinal voltage. (C/LM) 802.12-1995, 802.3u-1995
(3) The voltage common to all conductors of a group as measured between that group at a given location and an arbitrary reference (usually earth). (PE/SWG) C37.100-1992

common return A return conductor common to several circuits. *See also:* center of distribution. (PE/T&D) [10]

common spectrum multiple access (communication satellite) A method of providing multiple access to a communication satellite in which all of the participating earth stations use a common time-frequency domain. Signal processing is em-

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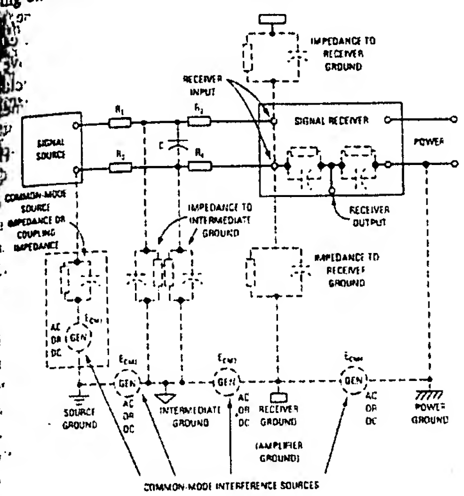

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Electronics/Nodal Analysis

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Nodes

A node is a section of a circuit which connects components to each other. All of the current entering a node must leave a node, according to Kirchoff's Current Law. Every point on the node is at the same voltage, no matter how close it is to each component, because the connections between components are perfect conductors. This voltage is called the node voltage, and is the voltage difference between the node and an arbitrary reference, the ground point. The ground point is a node which is defined as having zero voltage. The ground node should be chosen carefully for convenience. Note that the ground node does not necessarily represent an actual connection to ground, it is just a device to make the analysis simpler. For example, if a node has a voltage of 5 Volts, then the voltage drop between that node and the ground node will be 5 Volts.

Note that in real circuits, nodes are made up of wires, which are not perfect conductors, and so the voltage is not perfectly the same everywhere on the node. This distinction is only important in demanding applications, such as low noise audio, high speed digital circuits (like modern computers), etc.

Nodal Analysis

Nodal analysis is a formalized procedure based on KCL equations.

Steps:

1. Identify all nodes.
2. Choose a reference node. Identify it with reference (ground) symbol. A good choice is the node with the most branches, or a node which can immediately give you another node voltage (e.g., below a voltage source).
3. Assign voltage variables to the other nodes (these are node voltages.)
4. Write a KCL equation for each node (sum the currents leaving the node and set equal to zero).
   - Rearrange these equations into the form A*V1+B*V2=C (or similar for equations with more voltage variables.)
5. Solve the system of equations from step 4. There are a number of techniques that can be used: simple substitution, Cramer's rule, the adjoint matrix method, etc.

Complications in Nodal Analysis

1. Dependent Current Source
   Solution: Write KVL equations for each node. Then express the extra variable (whatever the

current source depends on) in terms of node voltages. Rearrange into the form from step 4 above. Solve as in step 5.

2. Independent Voltage Source

   Problem: We know nothing about the current through the voltage source. We cannot write KCL equations for the nodes the voltage source is connected to.

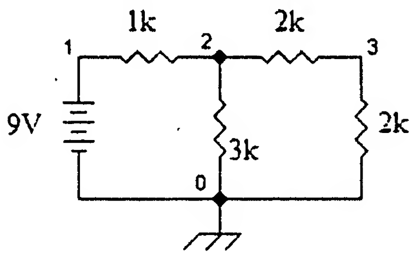
   Solution: If the voltage source is between the reference node and any other node, we have been given a 'free' node voltage: the node voltage must be equal to the voltage source value! Otherwise, use a 'super-node', consisting of the source and the nodes it is connected to. Write a KCL equation for all current entering and leaving the super-node. Now we have one equation and two unknowns (the node voltages). Another equation that relates these voltages is the equation provided by the voltage source (V2-V1=source value). This new system of equations can be solved as in Step 5 above.

3. Dependent Voltage Source

   Solution: Same as an independent voltage source, with an extra step. First write a super-node KCL equation. Then write the source controlling quantity (dependence quantity?) in terms of the node voltages. Rearrange the equation to be in the A*V1+B*V2=C form. Solve the system as above.

Example

Given the Circuit below, find the voltages at all nodes.



node 0: $V_0 = 0V$ (defined as ground node)

node 1: $V_1 = 9V$ (free node voltage)

node 2: $\dfrac{V_1 - V_2}{1k} = \dfrac{V_2 - V_0}{3k} + \dfrac{V_2 - V_3}{2k}$

node 3: $\dfrac{V_2 - V_3}{2k} = \dfrac{V_3 - V_0}{2k}$

which results in the following system of linear equations: $\begin{cases} +11V_2 & -3V_3 & = & 54 \\ +1V_2 & -2V_3 & = & 0 \end{cases}$

therefore, the solution is: $\begin{cases} V_0 = 0.00V \\ V_1 = 9.00V \\ V_2 = 5.68V \\ V_3 = 2.84V \end{cases}$

Another solution with KCL would be to solve node in terms of node 2;

$$\frac{V_2 - 9V}{1k} + \frac{V_2}{3k} + \frac{V_2}{4k} = 0$$